

CLAIMS:

What is claimed is:

- 1 1. A method of processing a bit transfer operation instruction, comprising:
 - 2 fetching and decoding a bit value transfer instruction;
 - 3 executing the bit value transfer instruction on a source bit position of a first data
 - 4 memory location to select a bit value in the source bit position of the first data memory
 - 5 location, the bit position of the first data memory location specified in the bit value transfer
 - 6 instruction;
 - 7 writing the value to a destination bit position of a second data memory location, the
 - 8 destination bit position specified in the bit value transfer instruction.
- 1 2. The method according to claim 1, wherein the step of executing the bit value transfer
- 2 instruction includes reading an operand at the first memory location.
- 1 3. The method according to claim 2, wherein the step of executing the bit value transfer
- 2 instruction includes copying the bit value at the source bit position of the operand.
- 1 4. The method according to claim 3, wherein the step of executing the bit value transfer
- 2 instruction includes writing the operand to the first memory location.
- 1 5. The method according to claim 4, wherein the bit value transfer instruction is a first
- 2 test bit value transfer instruction.

- 1 6. The method according to claim 5, wherein the first test bit value transfer instruction
2 specifies a carry status bit position as the destination bit position of the second memory
3 location.
- 1 7. The method according to claim 6, wherein the first test bit value transfer instruction
2 specifies a register as the first data memory location.
- 1 8. The method according to claim 6, wherein the first test bit value transfer instruction
2 specifies an address in data memory as the first data memory location.
- 1 9. The method according to claim 4, wherein the bit value transfer instruction is a second
2 test bit value transfer instruction.
- 1 10. The method according to claim 9, wherein the second test bit value transfer instruction
2 specifies a zero status bit position as the destination bit position of the second memory
3 location.
- 1 11. The method according to claim 10, wherein the second test bit value transfer
2 instruction specifies a register as the first data memory location.

- 1 12. The method according to claim 10, wherein the second test bit value transfer
2 instruction specifies an address in data memory as the first data memory location.
- 1 13. The method according to claim 1, wherein the step of executing the bit value transfer
2 instruction includes reading an operand at the second memory location.
- 1 14. The method according to claim 13, wherein the step of executing the bit value transfer
2 instruction includes copying the bit value at the source bit position of the first memory
3 location.
- 1 15. The method according to claim 14, wherein the step of executing the bit value transfer
2 instruction includes writing the operand to the second memory location.
- 1 16. The method according to claim 15, wherein the bit value transfer instruction is a first
2 write bit value transfer instruction.
- 1 17. The method according to claim 16, wherein the first write bit value transfer instruction
2 specifies a zero status bit position as the source bit position of the first memory
3 location.
- 1 18. The method according to claim 17, wherein the first write bit value transfer instruction
2 specifies a register as the second data memory location.

1 19. The method according to claim 17, wherein the first write bit value transfer instruction
2 specifies an address in data memory as the second data memory location.

1 20. The method according to claim 15, wherein the bit value transfer instruction is a
2 second write bit value transfer instruction.

1 21. The method according to claim 20, wherein the second write bit value transfer
2 instruction specifies a carry status bit position as the source bit position of the first
3 memory location.

1 22. The method according to claim 21, wherein the second write bit value transfer
2 instruction specifies a register as the second data memory location.

1 23. The method according to claim 21, wherein the second write bit value transfer
2 instruction specifies an address in data memory as the second data memory location.

1 24. A processor for bit transfer operation instruction processing, comprising:
2 a program memory for storing instructions including a bit value transfer operation
3 instruction;
4 a program counter for identifying current instructions for processing; and

5 an arithmetic logic unit (ALU) for executing instructions within the program
6 memory, the ALU including bit value transfer operation logic for executing the bit value
7 transfer operation instruction on a source bit position of a first data memory location to
8 select a bit value in the source bit position of the first data memory location, the bit
9 position of the first data memory location specified in the bit value transfer instruction and
10 writing the value to a destination bit position of a second data memory location, the
11 destination bit position specified in the bit value transfer instruction.

1 25. The processor according to claim 24, wherein the step of executing the bit value
2 transfer instruction includes the ALU reading an operand at the address in the first
3 memory location.

1 26. The processor according to claim 25, wherein the step of executing the bit value
2 transfer instruction includes the ALU copying the bit value at the source bit position of
3 the operand.

1 27. The processor according to claim 26, wherein the step of executing the bit value
2 transfer instruction includes the ALU writing the operand to the address in the first
3 memory location.

1 28. The processor according to claim 27, wherein the bit value transfer instruction is a first
2 test bit value transfer instruction.

1 29. The processor according to claim 28, wherein the first test bit value transfer instruction
2 specifies a carry status bit position as the destination bit position of the second memory
3 location.

1 30. The processor according to claim 29, wherein the first test bit value transfer instruction
2 specifies a register as the first data memory location.

1 31. The processor according to claim 29, wherein the first test bit value transfer instruction
2 specifies an address in data memory as the first data memory location.

1 32. The processor according to claim 27, wherein the bit value transfer instruction is a
2 second test bit value transfer instruction.

1 33. The processor according to claim 32, wherein the second test bit value transfer
2 instruction specifies a zero status bit position as the destination bit position of the
3 second memory location.

1 34. The processor according to claim 33, wherein the second test bit value transfer
2 instruction specifies a register as the first data memory location.

- 1 35. The processor according to claim 33, wherein the second test bit value transfer
2 instruction specifies an address in data memory as the first data memory location.
- 1 36. The processor according to claim 24, wherein the step of executing the bit value
2 transfer instruction includes the ALU reading an operand at the address in the second
3 memory location.
- 1 37. The processor according to claim 36, wherein the step of executing the bit value
2 transfer instruction includes the ALU copying the bit value at the source bit position of
3 the first memory location.
- 1 38. The method according to claim 37, wherein the step of executing the bit value transfer
2 instruction includes the ALU writing the operand to the address in the second memory
3 location.
- 1 39. The processor according to claim 38, wherein the bit value transfer instruction is a first
2 write bit value transfer instruction.
- 1 40. The processor according to claim 39, wherein the first write bit value transfer
2 instruction specifies a zero status bit position as the source bit position of the first
3 memory location.

- 1 41. The processor according to claim 40, wherein the first write bit value transfer
2 instruction specifies a register as the second data memory location.
- 1 42. The processor according to claim 40, wherein the first write bit value transfer
2 instruction specifies an address in data memory as the second data memory location.
- 1 43. The processor according to claim 38, wherein the bit value transfer instruction is a
2 second write bit value transfer instruction.
- 1 44. The processor according to claim 43, wherein the second write bit value transfer
2 instruction specifies a carry status bit position as the source bit position of the first
3 memory location.
- 1 45. The processor according to claim 44, wherein the second write bit value transfer
2 instruction specifies a register as the second data memory location.
- 1 46. The processor according to claim 44, wherein the second write bit value transfer
2 instruction specifies an address in data memory as the second data memory location.